UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,475	10/16/2003	Ronald G. Filippi JR.	YOR920030441US1 (163-14)	7958

24336 7590 11/27/2006

KEUSEY, TUTUNJIAN & BITETTO, P.C.
20 CROSSWAYS PARK NORTH
SUITE 210
WOODBURY, NY 11797

EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,475	FILIPPI ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/16/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/687,475 filed 10/16/2003 and amendment filed 09/06/2006.

2. Claims 1-32 remain pending in the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/06/2006 has been entered.

Claim Objections

4. Claims 11, 21, 30 are objected to because of the following informalities: it has to be noted that the status of claims 11, 21, 30 has an error: status was indicated as "Previously Presented" instead of "Currently Amended", since the amendment after Final was not entered as indicated in the Advisory Action mailed 08/08/2006.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Corson et al. (US Patent 6,629,292).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 1 Corson et al. teaches a method for analyzing circuit designs col. 1, ll.6-11; col. 4, ll.8-16), comprising the steps of: discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design (within a method for forming gray scale images in a semiconductor process (col. 4, ll.45-48) using pixel design schemes during semiconductor manufacturing process (col. 4, ll.63-65) and as shown on the Figs. 3a and 3b, wherein forming graphical images in semiconductor devices having plurality of pixel elements (col. 1, ll.6-12; col. 5, ll.10-18), and Figs. 4a and 4b showing pixel element representing the portion of the semiconductor device (col. 5, ll.47-54)); determining at least one property for each pixel element representing the portion of the design where the at least one property is represented by an intensity of the pixel

element, such that the pixel elements provide a pixel map to visually represent the design representation based on the at least one property (by measuring an intensity of the pixel element (col. 18, ll.40-46), including mapping of the gray scale images to a chip layout design (col. 6, ll.56-60; ll. 65-67) to visually represent the chip design by gray scale images within pixel elements (col. 7, ll.21-25)); and determining a response of the design due to local properties across the design based upon representations of the pixel elements (within forming gray level images in the surface of semiconductor device and converting this images into two dimensional pattern of contrasting materials (col. 1, ll.43-54)).

With respect to claim 13 Corson et al. teaches similar limitation as to claim 1 and further including: assembling pixel properties to determine properties of a local three-dimensional circuit architecture (within a method of forming graphical images (col. 1, ll.6-12) by using gray scale images firming with structures and techniques used in the fabrication of integrated circuits (col. 4, ll.8-16; ll.58-60) as shown on the Figs. 4a and 4b in multilayered semiconductor device (col. 5, ll.47-54)); and determining a global response of the circuit architecture due to local properties across the design (within forming gray level images in the surface of semiconductor device and converting this images into two dimensional pattern of contrasting materials (col. 1, ll.43-54)).

With respect to claim 23 Corson et al. teaches similar limitations as to claim 13 and further including: importing a digitally rendered representation of a design (col. 6, ll.12-23).

With respect to claim 32 Corson et al. teaches a method for analyzing circuit designs (col. 1, ll.6-11; col. 4, ll.8-16), comprising the steps of: discretizing a design representation into pixel elements representative of a structure in the design (within a method for forming gray scale images in a semiconductor process (col. 4, ll.45-48) using pixel design schemes during semiconductor manufacturing process (col. 4, ll.63-65) and as shown on the Figs. 3a and 3b, wherein forming graphical images in semiconductor devices having plurality of pixel elements (col. 1, ll.6-12; col. 5, ll.10-18), and Figs. 4a and 4b showing pixel element representing the portion of the semiconductor device (col. 5, ll.47-54)); determining at least one property for each pixel element representing a portion of the design wherein the at least one property includes metal fraction information relating to a metal fraction of structures in the portion (by measuring an intensity of the pixel element (col. 18, ll.40-46), including mapping of the gray scale images to a chip layout design (col. 6, ll.56-60; ll. 65-67) to visually represent the chip design by gray scale images within pixel elements (col. 7, ll.21-25), wherein the concept of different amount of reflected light from different materials, such as different level of metal M1 and M3, fir example, is used (col. 6, ll.1-8)); and determining a response of the design die to local properties across the design (within forming gray level images in the surface of semiconductor device and converting this images into two dimensional pattern of contrasting materials (col. 1, ll.43-54)).

With respect to claims 2-12, 14-22 and 24-31 Corson et al. teaches:

Claims 2, 14, 24: further comprising the step of exporting pixel properties to an application (col. 6, ll.56-67);

Claim 3: further comprising the step of assembling pixel properties to determine local three-dimensional properties (within a method of forming graphical images (col. 1, ll.6-12) by using gray scale images firming with structures and techniques used in the fabrication of integrated circuits (col. 4, ll.8-16; ll.58-60) as shown on the Figs. 4a and 4b in multilayered semiconductor device (col. 5, ll.47-54));

Claim 4: wherein the step of determining a response of the design due to local properties across the design includes the step of determining a global response for an architecture due to the local three-dimensional properties (within forming gray level images in the surface of semiconductor device and converting this images into two dimensional pattern of contrasting materials (col. 1, ll.43-54));

Claims 5, 15: further comprising the step of importing a design to be analyzed (col. 6, ll.12-23; col. 14, ll.14-25);

Claims 6,16, 25: wherein the design includes a computer generated design of one of a circuit and a chip (col. 14, ll.14-25);

Claims 7, 17, 26: wherein the at least one property includes metal fraction and the global response includes thermal strain (col. 6, ll.1-8);

Claims 8, 18, 27: wherein the step of determining a response of the design includes accepting or rejecting a design based on the response (col. 20, ll.51-67);

Claims 9, 19, 28: further comprising the step of altering a design based on the response (col. 20, ll.51-67);

Claims 10, 20, 29: wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image (col.1, ll.50-54; col. 5, ll.47-54);

Claims 11, 21, 30: a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing circuit designs, as recited in claim 1 (col. 14, ll.14-25);

Claims 12, 22, 31: wherein the at least one property includes metal fraction information relating to the metal fraction is generated for the location and number of stacked via structures (col. 6, ll.1-8; col. 17, ll.11-17).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Rossoshek
Examiner
Art Unit 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER